Carl Anderson

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Education

University of Minnesota Twin Cities, Minneapolis MN

Master of Science in Electrical and Computer Engineering *Expected May 2024*
GPA: 3.81/4.00

Bachelor of Computer Engineering *May 2023*
GPA: 3.75/4.00 | Dean's List Fall | IEEE HKN Member
Related Coursework: VLSI Digital Signal Processing, Stochastic Processes, VLSI Design, Algorithms

Skills

Tools: Xilinx Vivado, Git, Jira, Confluence, Jenkins, MATLAB, Mathematica, Altium Designer, Synopsys [Verdi, HSPICE, Cosmoscope, Design Compiler, VCS], Cadence [Genus, Innovus, Virtuoso], Calibre [DRC, LVS, PEX]

Languages: Python, C, C++, Verilog, SystemVerilog, TCL, Bash, Java

Exposures: RTL design for FPGA, 7nm FinFET CMOS circuit design, Design verification w/ DFT, Deeply pipelined computer architectures, Deep Learning in Pytorch, Formal Equivalence with Synopsys Verdi, Firmware programming on FreeRTOS platforms, Signal processing for sensor fusion systems, Linux scripting and automation

Work Experience

RTL Design Intern, Advanced Micro Devices *January 2023 – August 2023*
- Worked on load/store unit in next generation high performance x86 CPU core
- Designed RTL structures in SystemVerilog and performed verification using Synopsys Verdi
- Used formal equivalence flow for RTL changes to support physical design power & timing

Graduate Teaching Assistant, Intro to C++ *August 2023 – Present*
- Guided students through hands-on practical exercises to reinforce key programming principles in C++ such as memory management, pointers, and basic algorithms
- Taught basic digital microcontroller coding and wiring principles for internet of things project

Firmware Engineering Intern, Hewlett Packard Enterprise, Bloomington MN *May 2021 – August 2022*
- Developed JTAG drivers to perform DFT functions for ASIC bringup including MBIST, ALLSCAN, and clock observation on next-gen networking ASIC for high performance computing (HPC) systems
- Wrote device driver firmware in C for FreeRTOS platform to maintain system stability for Slingshot high performance network devices
- Developed Python regression software for HPC systems to track performance over time and detect faults

Activities

Avionics Lead, University of Minnesota Rocket Team *May 2021 – August 2023*
- Lead team of 15 with annual budget of $3,300 in design & construction of reusable flight computer project for data collection in high power sounding rocket flights
- Organized cross-team integrations such as pitot probes, active controls, and sensor filtering algorithms
- Led team in design and operation of student made radar & custom GPS receiver for rocket apogee determination
- Wrote accessible technical documentation for competition report to maximize comprehensibility for team & judges

Avionics Hardware Lead, University of Minnesota Rocket Team *August 2019 – May 2021*
- Designed schematics and PCB layout for on-board flight computer card stack in Altium
- Assembled SMD PCBs using reflow soldering and tested for manufacturing & design issues
- Wrote firmware for serial communication via SPI and UART between microcontrollers and sensors in C

Research

Undergraduate Research Assistant, University of Minnesota *August 2021 – Present*
Professor Keshab Parhi, Department of Electrical and Computer Engineering

Hyperdimensional Computing
- Developed hybrid hyperdimensional computing-deep learning models for multivariate anomaly detection
- Improved accuracy by 1.11% and sensitivity by 4.88% over current state-of-the-art methods

Molecular MUX Physical Unclonable Functions
Presented at 2023 IEEE International Midwest Symposium on Circuits and Systems *August 2023*
- Designed stochastic (soft) molecular MUX physical unclonable function (PUF) using fractional coding
- Ran simulations in Mathematica to determine viability of soft molecular MUX PUF for bio-security applications

Undergraduate Research Opportunities Program *Spring 2022*
- Designed and characterized stochastic physical unclonable functions for use in low energy hardware security applications and presented findings in research symposium

Projects

Hierarchical Re-reference Interval Prediction (HRRIP) Caching Policy – Advanced Computer Architecture *Fall 2023*
- Developed new cache replacement policy based on RRIP which utilizes layered values to deliver up to 8% IPC uplift with a 30% decrease in hardware overhead
- Used ChampSim to gather metrics vs other policies across a number of benchmarks and configurations

Analytic Placement – VLSI Design Automation *Fall 2023*
- Designed physical cell placement engine in C++ for use in large-scale VLSI chips
- Implemented quadratic placement using gradient descent & cell spreading based on FastPlace (2005) paper and tested on IBM standard cell benchmarks

Static Timing Analysis – VLSI Design Automation *Fall 2023*
- Implemented NLDM-based STA engine in C++ for critical path & slack analysis and ran on ISCAS 89/99 circuits

Universal Flight Computer Architecture – Rocket Team *Summer 2023*
- Architected second version of modular flight computer system, including complete uC platform swap
- Focused on easing debug and bring-up by adding hardware test-points and software debug ports to enable future hardware-in-the-loop testing

Pitot Tube Airspeed and Angle of Attack Determination using Deep Learning – Rocket Team *Spring 2023*
- Designed DL model for trans/supersonic airspeed and angle of attack determination with very limited dataset size
- Achieved model errors of <0.035 Mach & <0.48 degrees using dataset augmentation & hyperparameter tuning

High-Speed CMOS Ising Machine Testing Platform – Sr. Design *Spring 2023*
- Lead team of 5 by managing team workload, communicating with sponsor, and ensuring timely completion
- Wrote RTL for Zync SoC which drove ising machine chips & software interface to FPGA
- Delivered 366x higher throughput and 98.59% energy savings vs. previous generation

Parameterized Matrix-Matrix Multiplication Systolic Array – VLSI Design Lab *Fall 2022*
- Designed configurable systolic array of multiply-accumulate nodes in Verilog RTL for machine learning accelerator
- Theoretical throughput of 1264 giga-integer operations per second

Digitally Controlled Oscillator – VLSI Design I *Fall 2022*
- Designed RTL, performed synthesis and automatic placement & routing using Cadence Genus and Innovus tools
- Ran simulations for determining power consumption and output reliability using HSPICE

Deep Learning Segmentation of White Matter Lesions from Brain MRI – Deep Learning *Fall 2022*
- Compared models for the task of segmenting Alzheimers-linked lesions in brain MRIs
- Utilized transfer learning on previously unused dataset to achieve Dice loss of <0.135

Spiking Neural Network Research Paper – VLSI Digital Signal Processing *Spring 2022*
- Completed research paper covering past and recent developments on spiking neural networks including model training optimization, implementation, and mapping onto dedicated neuromorphic hardware